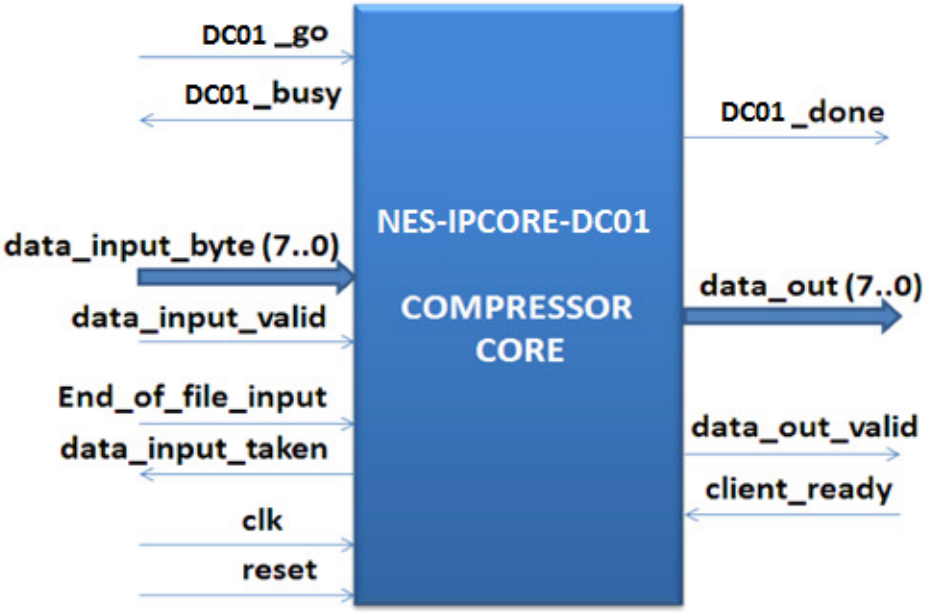
NES-IPCORE-DC01
Data Compression IP CORE

// OVERVIEW

Implements the compression algorithm Lempel-Ziv Ross William version 3,
Process data at the speed of 1 Gbps (with an input clock of 125 MHz),
Support variety of data blocks of 2KB – 32KB,
The compression ratio greatly depends on the data; on typical file corpuses varies between 1.5 and 2,
Relay on the FPGA's internal memory alone, without any interface with outer memory resources.



// HIGHLIGHTS

The NES- IPCORE-DC01 is designed for high speed data compression requirements it compresses at speed rate of 1GB/s the NES- IPCORE-DC01core inputs the data file and other functional ports and outputs the compressed file, works on frequency of 125 Mhz in both sides (Input/output ports).

INPUTS		
Signal name	**Width (bits)**	**Description**
Clk	1	System clk
Reset	1	System reset
DC01_go	1	'1' for start compression operation
Data_input_byte	8	Core raw data input, one byte per clock
Data_input_valid	1	When '1' – input is valid
End_of_file_input	1	When '1' - raw data insertion is over
Client_ready	1	When '1' - Client is ready to receive compressed data
OUTPUTS		
Data_input_taken	1	Indicate that input data is taken
Data_out	8	Core data output
Data_out_valid	1	data_out is valid – '1'
DC01_done	1	When '1'- Indicate to client that compression and send operations are finish
DC01_busy	1	Core ready to receive input data – '0' Core busy (sending data out) – '1'